DFXO

LVDS - LVPECL & CMOS Output

20 MHz to 300 MHz

Differential Output Crystal Oscillator

DESCRIPTION

Statek's 5 mm x 7 mm surface mount Differential Output Crystal Oscillator is designed for applications requiring low jitter and ultra high frequency differential outputs in a small footprint. Offered at frequencies from 20 MHz to 300 MHz with operation over a temperature range of (-40°C to +105°C). No external decoupling capacitor required with internal capacitor.

FEATURES

- LVDS - LVPECL- CMOS outputs available
- Low phase noise - Low phase jitter
- Internal 0.01µF SMD decoupling capacitor
- Low Allan deviation
- High Frequency Fundamental Mode Crystal
- Extended Industrial temperature range

APPLICATIONS

Military & Aerospace

- Avionics
- Communications
- Networking

TERMINATIONS

Designation	Termination
SM1	Gold Plated (Pb Free)
SM3	Solder Dipped
SM5	Solder Dipped (Pb Free)

ENABLE/DISABLE OPTIONS (T/N)

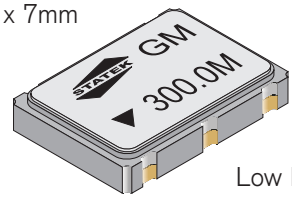
Statek offers two enable/disable options: T and N. The T-version has a Tri-State output and continues to oscillate internally when the output is put into the high Z state. As a result, when re-enabled, the oscillator does not have to restart and an output with a stable frequency resumes almost immediately. The N-version does not have PIN 2 connected internally and so has no enable/disable capability. The following table describes the Enable/Disable option T.

ENABLE/DISABLE OPTION T FUNCTION TABLE

	Enable (PIN 1 High*)	Disable (PIN 1 Low)
Output	Frequency Output	High Z State
Oscillator	Oscillates	Oscillates
Current	Normal	Lower than normal

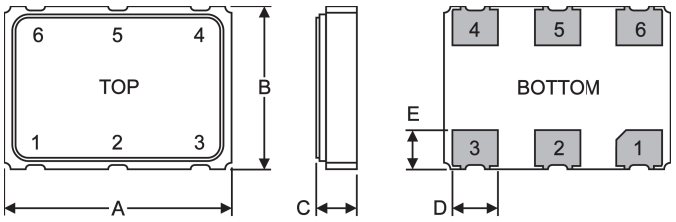
*When PIN 1 is allowed to float, it is held high by an internal pull-up resistor.

5mm x 7mm



Low Profile

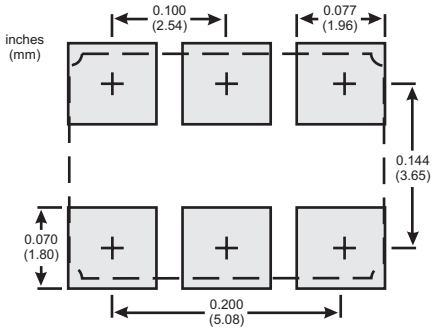
DIMENSIONS



PACKAGE DIMENSIONS

Dimension	Minimum mm	Typical mm	Maximum mm
A	6.86	7.00	7.16
B	4.85	5.00	5.16
C (SM1)	1.55	1.75	1.95
C (SM3/SM5)	1.65	1.85	2.05
D	1.19	1.40	1.41
E	1.07	1.27	1.47

SUGGESTED LAND PATTERN



PIN CONNECTIONS

1. (T) Enable/Disable or not connected (N)
2. (NC) Not Connected
3. Ground
4. LVDS - LVPECL - CMOS
5. LVDS - LVPECL (complementary)
6. Supply Voltage (V_{DD})

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD}	-0.5 V to 4.6 V
Storage Temperature	-65°C to +150°C
Maximum Process Temperature	260°C for 10 seconds
ESD Protection Human Body Model	2kV

PACKAGING OPTIONS

DFXO - Tray Pack

- Tape and reel Per EIA 481

SPECIFICATIONS

Nominal Frequency	20 MHz to 300 MHz
Operating Temperature[1]	-40°C to +85°C
Supply Voltage[2]	3.3V ±10% (2.5 V ±10% Available)
Shock, survival	5,000 g, 0.3 ms, ½ sine
Vibration, survival[6]	20 g, 10-2,000 Hz swept sine

SPECIFICATIONS TABLE

Parameters listed are at 25°C unless otherwise noted.

Parameter	Symbol	Units	Tightest	Standard	Maximum	Conditions / Comments
Frequency Stability[3]		PPM	±75	±100	±150	-40°C to +105°C
		PPM	±25	±50	±100	-40°C to +85°C
Aging		PPM		±5		First year depending on frequency
Calibration Tolerance[4]		PPM	±25	±50	±100	@25°C Other tolerances available
Frequency Tolerance (Total)		PPM	±25	±50	±100	-40°C to +85°C
LVDS Output Parameter	**Symbol**	**Units**	**Minimum**	**Typical**	**Maximum**	**Conditions / Comments**
Output Differential Voltage	V_{OD}	mV	247	355	454	RL = 100 Ω (See Figure 2)
V_{DD} Magnitude Change	ΔV_{OD}	mV	-50		50	
Output High Voltage	V_{OH}	V		1.4	1.6	
Output Low Voltage	V_{OL}	V	0.9	1.1		
Offset Voltage	V_{OS}	V	1.125	1.2	1.375	
Offset Magnitude Change	ΔV_{OS}	mV	0	3	25	
Power-off Leakage	I_{OXD}	uA		±1	±10	V_{OUT}=V_{DD} or GND (V_{DD} = 0V)
Short Circuit Current (Output)	I_{OSD}	mA		-6	-8	
Rise Time (Differential Clock)	t_R	nS	0.2	0.7	1	R_L =100 Ω 20% to 80% (See Figures 3 & 4)
Fall Time (Differential Clock)	t_F	nS	0.2	0.7	1	
Supply Current (Outputs Loaded)	IDD	mA		30*	80	* Typical for 125 MHz
Duty Cycle (Output Clock)[5]		%	40		60	@ 1.25 V
LVPECL Output Parameter	**Symbol**	**Units**	**Minimum**	**Typical**	**Maximum**	**Conditions / Comments**
Output High Voltage			V_{DD}-1.025			R_L =50 Ω to (V_{DD}-2V) (See Figure 5)
Output Low Voltage					V_{DD}-1.620	
Rise Time	t_R	nS		0.6	1.5	20% to 80% (See Figure 6)
Fall Time	t_F	nS		0.5	1.5	20% to 80% (See Figure 6)
Supply Current (Outputs Loaded)	IDD	mA			100	
Duty Cycle (Output Clock)[5]		%	40		60	@ V_{DD}-1.3V
CMOS Output Parameter	**Symbol**	**Units**	**Minimum**	**Typical**	**Maximum**	**Conditions / Comments**
Short Circuit Current		mA		±50		
Output Drive Current (CMOS)	I_{OH}	mA	20	25		V_{OH}=V_{DD}-0.4V, V_{DD}=3.3V
	I_{OL}	mA	20	25		V_{OL}=0.4V, V_{DD}=3.3V
Rise/Fall Time (CMOS)	$t_r t_f$	nS		1.5		10% to 90% 3.3V, 15pF
Output Load (CMOS)	CL	pF			15	(See Figure 1)
Supply Current (Outputs Loaded)	IDD	mA			40	200 MHz Maximum
Duty Cycle (Output Clock)[5]	%		40		60	@ 50% V_{DD}
Timing Jitter						
Jitter (Integrated) (LVDS)		pS		0.3	0.4	125 MHz (12 kHz to 20 MHz RMS)
Jitter (Period) (LVDS)		pS		2.0		125 MHz (10,000 cycles RMS)
Phase Noise - 125 MHz	Offset Frequency		@ 10 Hz	@ 100 Hz	@ 1 kHz	@ 10 kHz / @ 100 kHz
Typical (LVDS)	$\mathcal{L}(f)$ dBc/Hz		-85	-110	-133	-143 / -148

1. -40°C to +105°C at selected frequencies. Please contact factory.
2. 2.5 V available for frequencies up to 160 MHz.
3. Does not include calibration tolerance.
4. Contact factory for tighter tolerance.
5. Contact factory for 45/55% duty cycle.
6. Per MIL-STD-202G, Method 204D, Random vibration testing also available.

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HOW TO ORDER DFXO SURFACE MOUNT CRYSTAL OSCILLATORS

DFXO — C — 4 — T — SM3 — — 300.0M , 50 / 50 / — / I

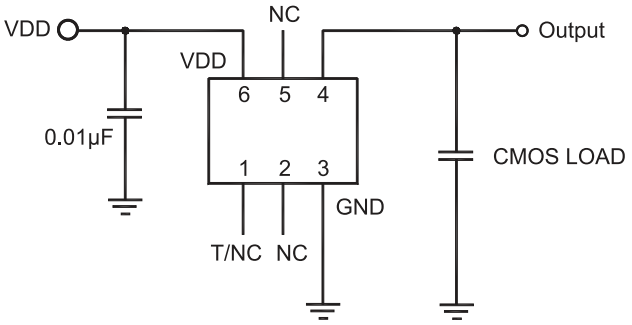
- **C** — Output Type: C = CMOS; D = LVDS; P = LVPECL
- **4** — Supply Voltage: 2 = 2.5 V; 4 = 3.3 V
- **T** — Enable/Disable Option T or N
- **SM3** — Terminations: Blank = SM1; = Gold Plated (Pb Free); SM3 = Solder Dipped; SM5 = Solder Dipped (Pb Free)
- **300.0M** — Frequency: M = MHz
- **50** — Calibration Tolerance @ 25°C (in ppm)
- **50** — Frequency Stability over Temp. Range (in ppm)
- **I** — Temperature Range: C = -10°C to +70°C; I = -40°C to +85°C; E = -40°C to +105°C; S = Customer Specified

OR

— / — / 100 / I

- **100** — Total Frequency Tolerance (in ppm)
- **I** — Temperature Range: C = -10°C to +70°C; I = -40°C to +85°C; E = -40°C to +105°C; S = Customer Specified

CMOS Test Circuit



Note: a 0.1µF bypass capacitor between VDD and GND pins as close as possible is recommended to minimize power supply line noise.

Figure 1

LVDS Levels Test Circuit

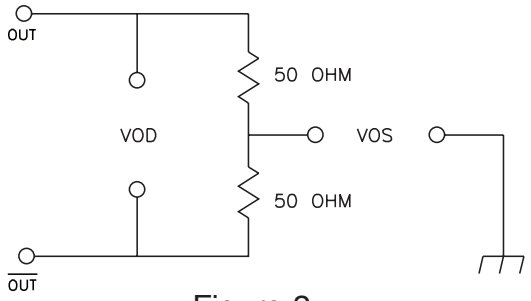


Figure 2

LVDS Switching Test Circuit

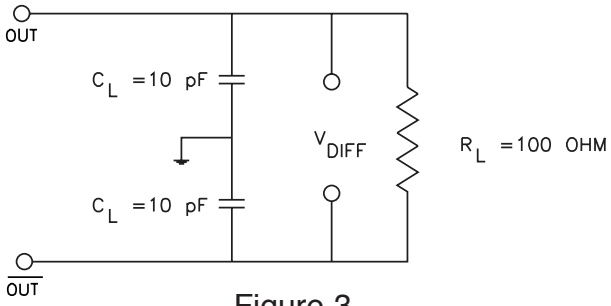


Figure 3

LVDS Transition Time Waveform

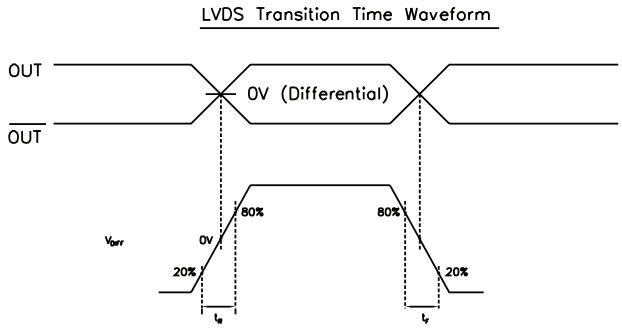


Figure 4

LVPECL Levels Test Circuit

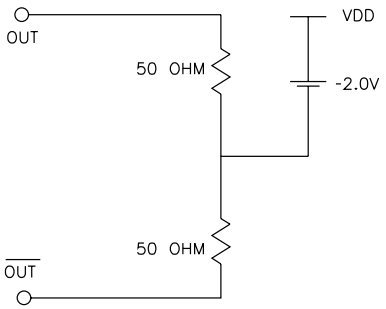
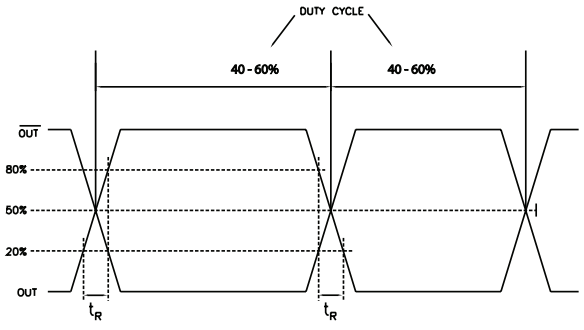


Figure 5



LVPECL Transition Time Waveform

Figure 6

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